UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/613,331	07/07/2000	MASAMOTO TAGO	WN-2205	9072

466 7590 07/23/2004

YOUNG & THOMPSON
745 SOUTH 23RD STREET 2ND FLOOR
ARLINGTON, VA 22202

EXAMINER	
HOANG, QUOC DINH	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/613,331	TAGO ET AL.	
	Examiner	Art Unit	
	Quoc D Hoang	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-34,45 and 47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25,27,29-34,45 and 47* is/are rejected.

7)☒ Claim(s) *26 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, claims 25-34, 45 and 47 in the reply filed on 01/08/2004 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 25, 27, 29-34, 45 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saitou et al., (U.S. Pat 5,162,240) ("Saitou") and in view of Watanabe et al., (U.S. Pat 6,278,148) ("Watanabe").

Regarding claims 25, 32-34, and 47, Saitou., Figures. 1- 13, and related text on col. 1-20 which discloses a system semiconductor device comprising: a system LSI cell portion 30 (col. 16, lines 1-55 and Fig. 13); a global wiring layer 20 which at least has conductor means formed in a substrate 10 and a wiring layer of a single-layer or a multi-layer structure formed on the conductor means and which is laminated with the system LSI cell portion 30; the global wiring layer 20 comprises; first wiring layer formed on the semiconductor substrate 10, an insulating layer formed on the first wiring layer, a second wiring layer formed on the insulating layer, a first via which is formed in the insulating layer and which electrically connects the first wiring layer with the second wiring layer, and a second a second via which is buried the semiconductor

substrate 10 and which is electrically connected the first wiring layer and which serves as en electrode for an external circuit, the global wiring layer 20 being laminated with the system portion 30 by electrically connecting the LSI 30 with the second wiring layer through the pads so that the LSI 30 is electrically connected to the external circuit through the first wiring layer and the second wiring layer (col. 16, lines 1-55 and Fig. 13).

Saitou does not clearly disclose LSI which includes a plurality of functional blocks for realizing specific functions and which has pads formed on the functional blocks, each of the functional blocks serving as a unit circuit and being arranged on a semiconductor chip.

Regarding claims 25, 32-34, and 47, Watanabe teaches a LSI which includes a plurality of functional blocks for realizing specific functions and which has pads formed on the functional blocks, each of the functional blocks serving as an unit circuit and being arranged on a semiconductor chip (see col. 2, lines 27-41, col. 5, lines 6-65 and Fig. 4). At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the functional blocks teaching of Watanabe with Saitou's LSI cell portion because it would have increased the chip area as taught by Watanabe, column 1, lines 15-37.

Regarding claims 27 and 29, Saitou teaches inner bumps formed on a surface of the second wiring layer, and a secondary wring layer as the conductor means formed in the substrate 10 made of an organic material (see Fig. 13).

Regarding claims 30 and 45, Saitou teaches wherein a gap is present between the global wiring layer 20 and a circuit surface of the LSI cell portion 30 connected by the inner bump (see Fig. 13).

Regarding claim 31, Saitou teaches wherein a bump 14 which is arranged on a surface substrate 10 on the side wherein the wiring layer is not formed (see Fig. 1).

Allowable Subject Matter

4. Claims 26 and 28 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: Claims 26 and 28 recite, inter alia, a system semiconductor device, wherein the global wiring layer has a secondary wiring layer as the conductor means formed in the substrate made of an organic material, a first wiring layer formed on the secondary wiring layer, an insulating layer formed on the first wiring layer, a second wiring layer formed on the insulating layer and electrically connected to the first wiring layer through a via, and an adhesive layer formed on the insulating layer in an area where the second wiring layer is not formed. The art of record does not discloses or anticipate the above limitation in combination with other claim elements nor would be obvious to modify the art of record so as to from a device including the above limitation.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quoc Hoang whose telephone number is (571) 272-

1780. The examiner can normally be reached on Monday-Friday from 8.00 AM to 5.00 PM.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone numbers of the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Quoc Hoang
Patent examiner/AU 2818.

David Nelms
Supervisory Patent Examiner
Technology Center 2800